AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1.   (PREVIOUSLY PRESENTED) A method for verification, comprising the steps of:

(A)   generating one or more analog signals utilized by an analog design;

(B)   generating one or more source signals by adding a digital signature to each of said analog signals; and

(C)   modeling said analog design using said source signals in place of said analog signals for verifying connectivity.

2.   (PREVIOUSLY PRESENTED) The method according to claim 1, wherein step (C) further comprises the step of:

performing one or more simulations of said analog design with said source signals propagating through said analog design.

3.   (PREVIOUSLY PRESENTED) The method according to claim 1, wherein each of said digital signatures corresponds to a type of said analog signals having a predetermined parameter.

4.   (PREVIOUSLY PRESENTED) The method according to claim 1, wherein each of said digital signatures comprises a unique pulse width.

2

5.   (PREVIOUSLY PRESENTED) The method according to claim 1, further comprising the step of:

performing verification of said analog design.

6.   (PREVIOUSLY PRESENTED) The method according to claim 2, wherein performing said simulations further comprises the sub-step of:

verifying a connectivity of said analog signals through

5   said analog design.

7.   (PREVIOUSLY PRESENTED) The method according to claim 2, wherein performing said simulations further comprises the sub-step of:

verifying a model of an analog block within said analog

5   design configured to receive at least a particular one of said analog signals.

8.   (PREVIOUSLY PRESENTED) The method according to claim 7, wherein verifying said model further comprises the sub-step of:

verifying an output signal of said analog block for said digital signature associated with said particular one of said

5   analog signals.

9.   (PREVIOUSLY PRESENTED) A method for testing a model of an analog device, comprising the steps of:

(A)   generating one or more attributed signals each (i) having a unique digital signature and (ii) presented by a source block within said model of said analog device; and

(B)   verifying connectivity of said attributed signals to a destination block within said model of said analog device by verifying reception of said unique digital signatures associated with each of said attributed signals at said destination block.

10.   (PREVIOUSLY PRESENTED) The method according to claim 9, further comprising the step of:

disabling processing of a particular one of said attributed signals if said particular signal is not verified at said destination block.

11.   (PREVIOUSLY PRESENTED) The method according to claim 9, further comprising the step of:

verifying a model of said destination block configured to receive at least one of said attributed signals.

12.   (CANCELED)

13.   (CANCELED)

14.   (CANCELED)

15.   (CANCELED)

4

16.   (CANCELED)

17.   (CANCELED)

18.   (CANCELED)

19.   (CANCELED)

20.   (CANCELED)

21.   (PREVIOUSLY PRESENTED) The method according to claim 1, wherein each of said digital signatures comprises a plurality of pulses.

22.   (PREVIOUSLY PRESENTED) The method according to claim 1, wherein each of said digital signatures comprises a varying frequency signal.

23.   (PREVIOUSLY PRESENTED) A system comprising:

a source for a plurality of signals, at least one of said signals representing an analog signal having a digital signature; and

5   a simulator connected to said source and configured to (i) simulate an analog design, (ii) receive said signals and (iii)

5

verify a connectivity of said analog signal in said analog design using said digital signature.

24. (PREVIOUSLY PRESENTED) The system according to claim 23, wherein said source comprises an analog source block configured to generate said analog signal.

25. (PREVIOUSLY PRESENTED) The system according to claim 24, wherein said source further comprises an adder block configured to (i) generate said digital signature and (ii) add said digital signature to said analog signal.

26. (PREVIOUSLY PRESENTED) The system according to claim 25, wherein said source further comprises a digital source block configured to generate at least one of said signals representing a digital signal.

27. (PREVIOUSLY PRESENTED) The system according to claim 23, wherein said digital signature comprises a plurality of pulses.

28. (PREVIOUSLY PRESENTED) The system according to claim 27, wherein said pulses have a unique width to identify said analog signal.

29. (PREVIOUSLY PRESENTED) The system according to claim 27, wherein said digital signature has a varying frequency.

6